

FIG. I PRIOR ART

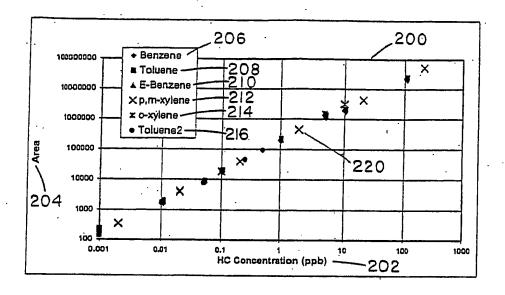


FIG. 2 PRIOR ART

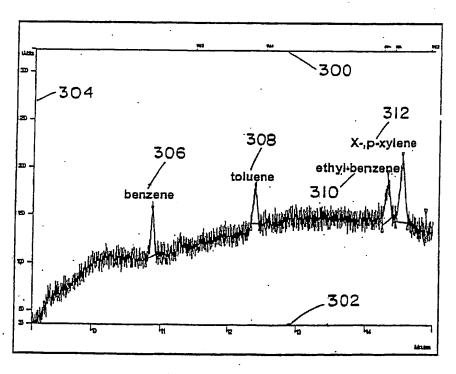


FIG. 3 PRIOR ART

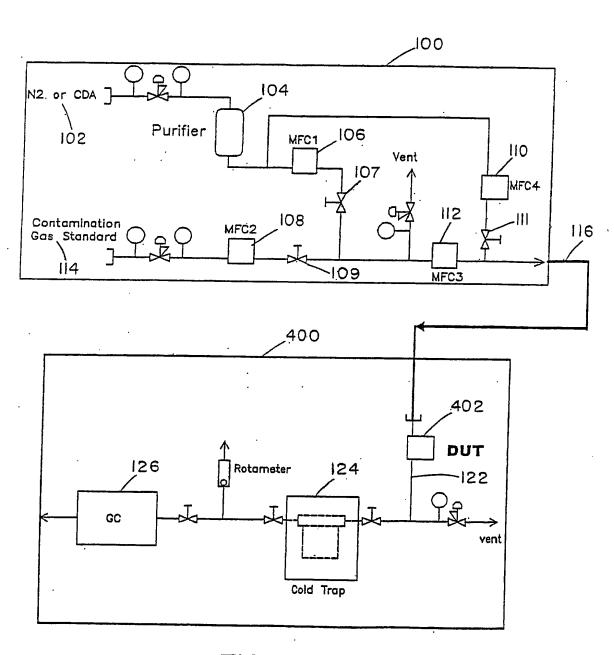
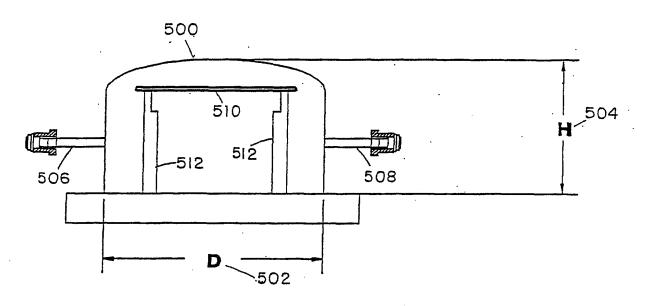
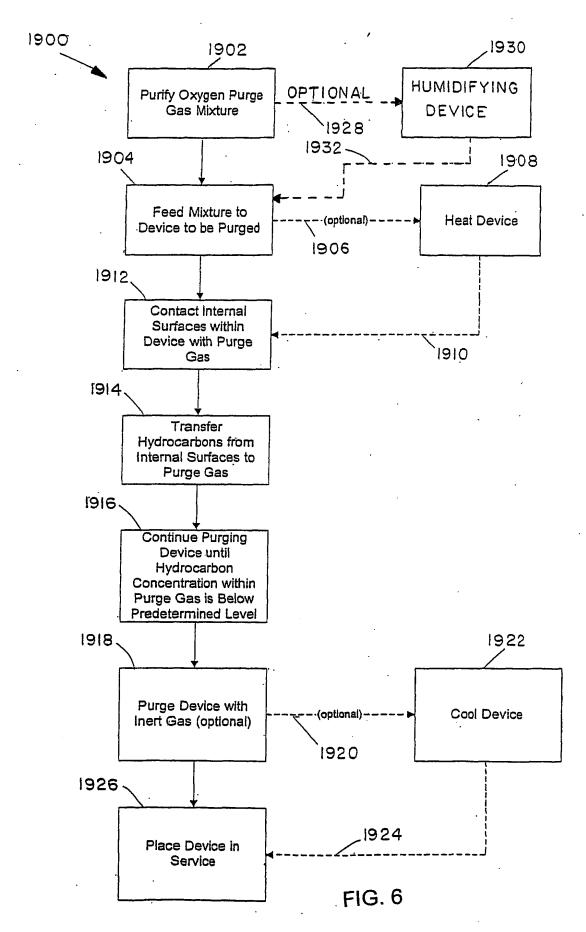


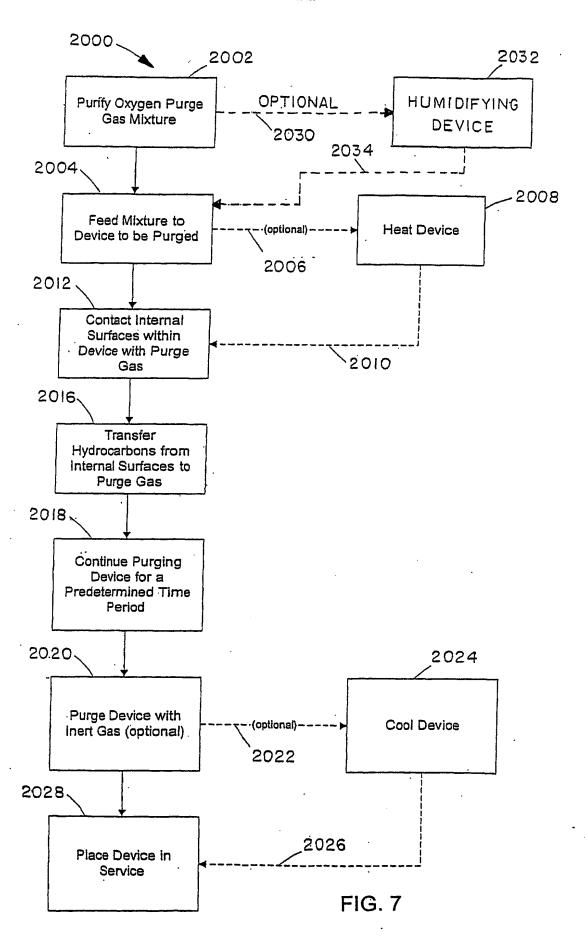
FIG.4

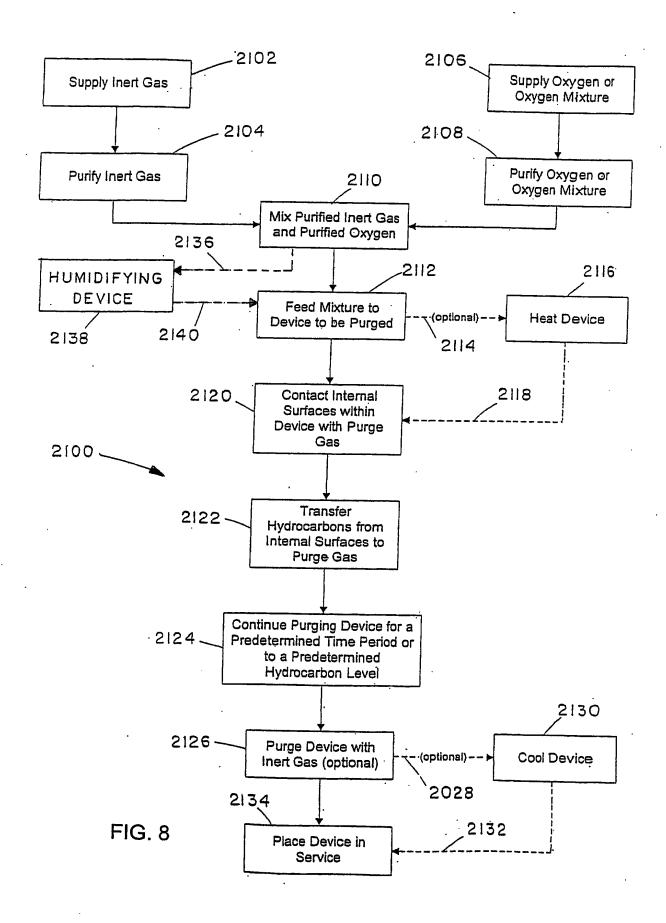


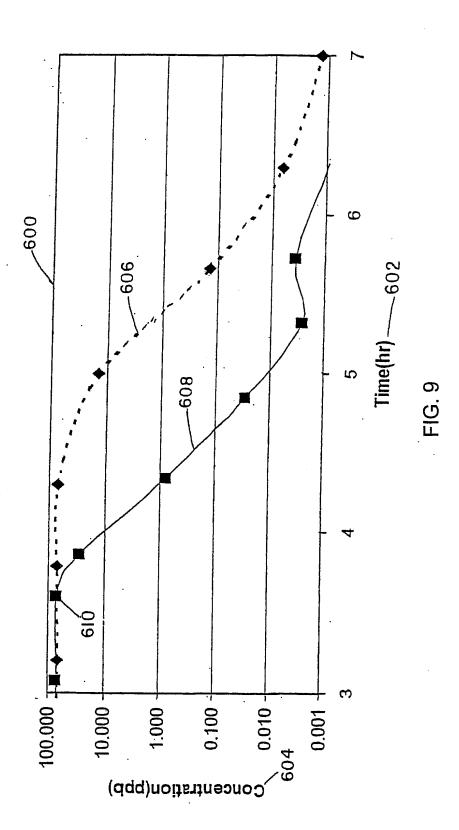
Wafer Chamber

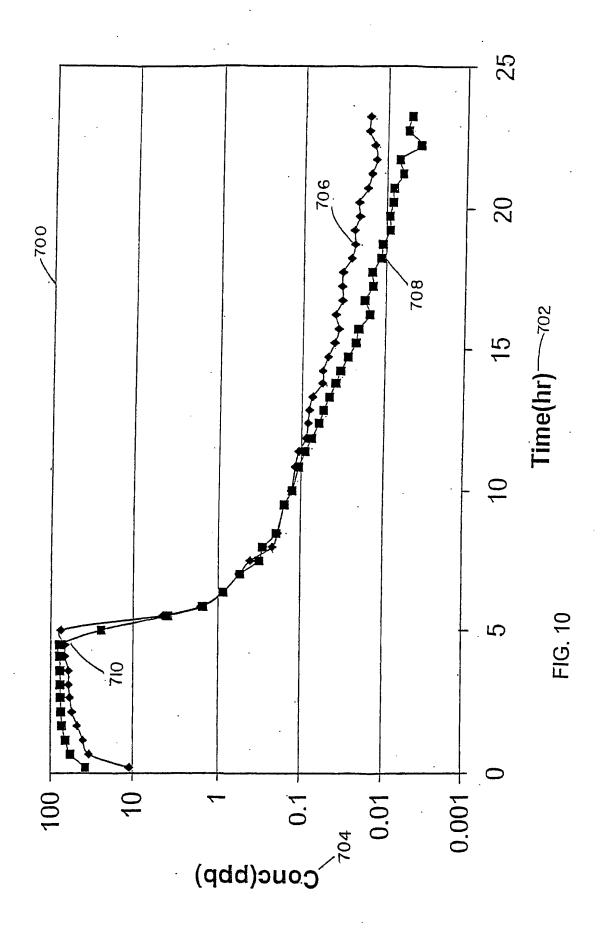
FIG. 5

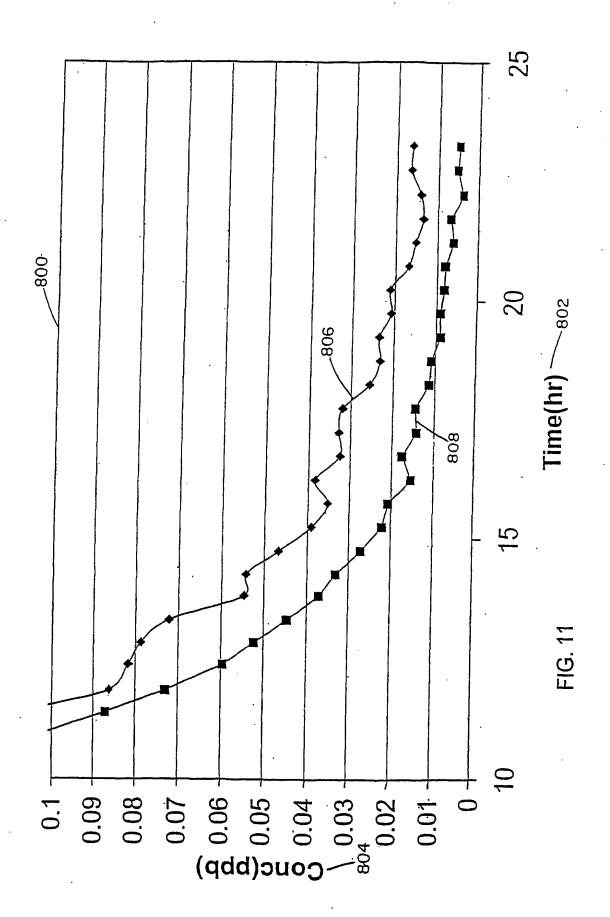


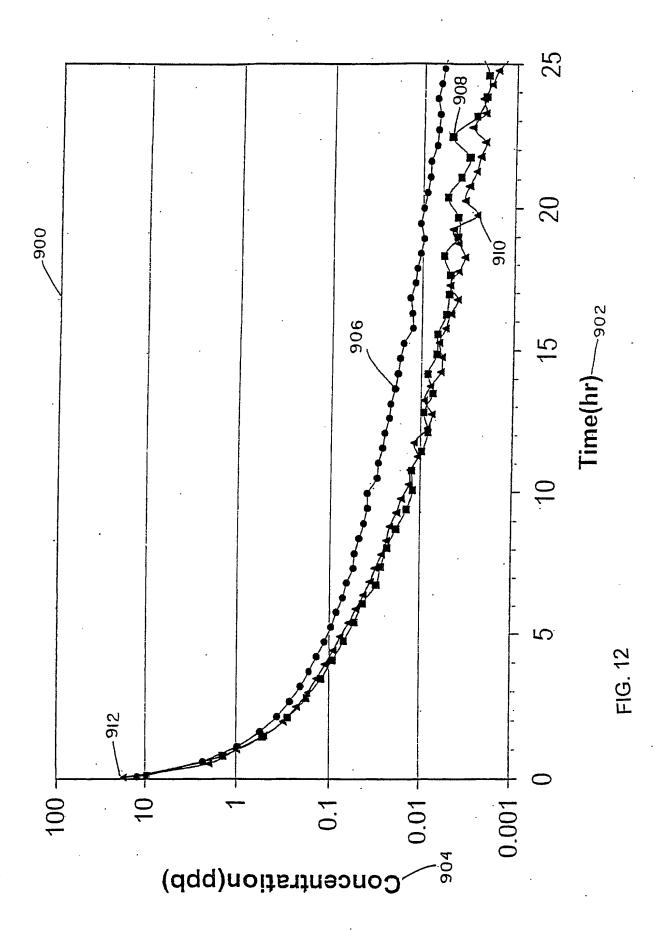


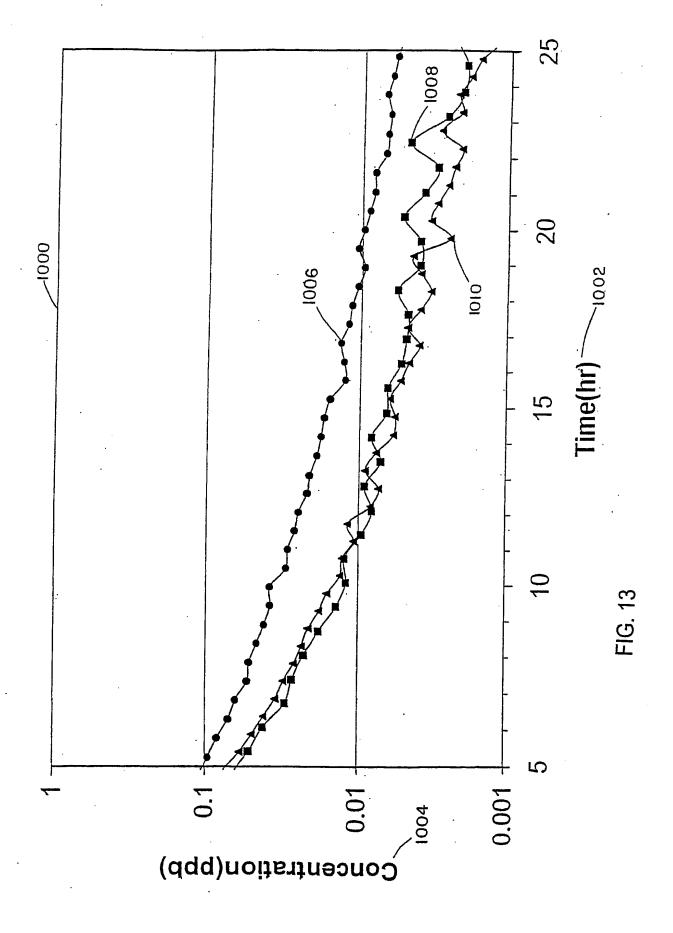


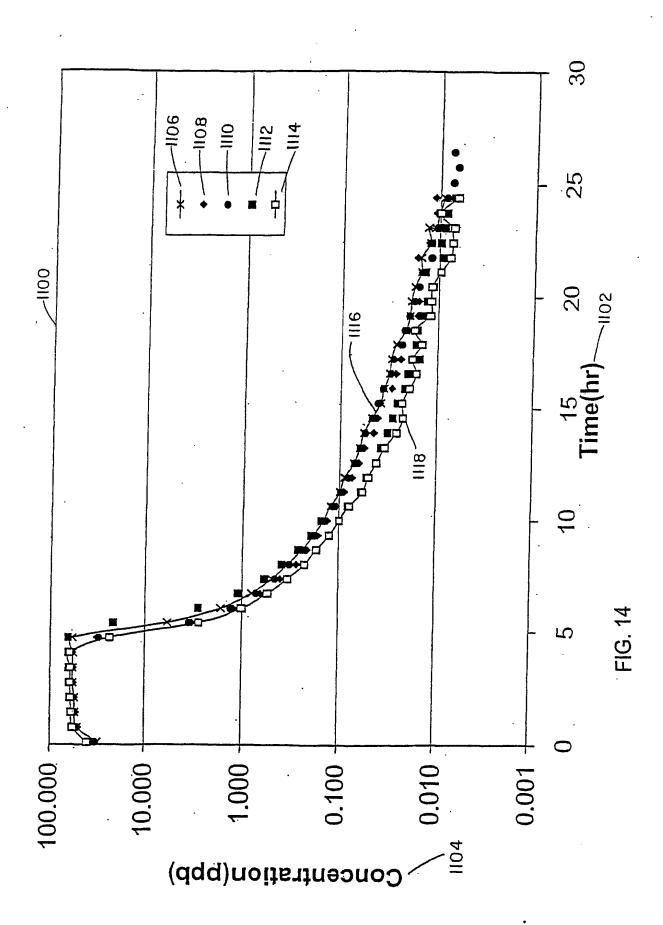


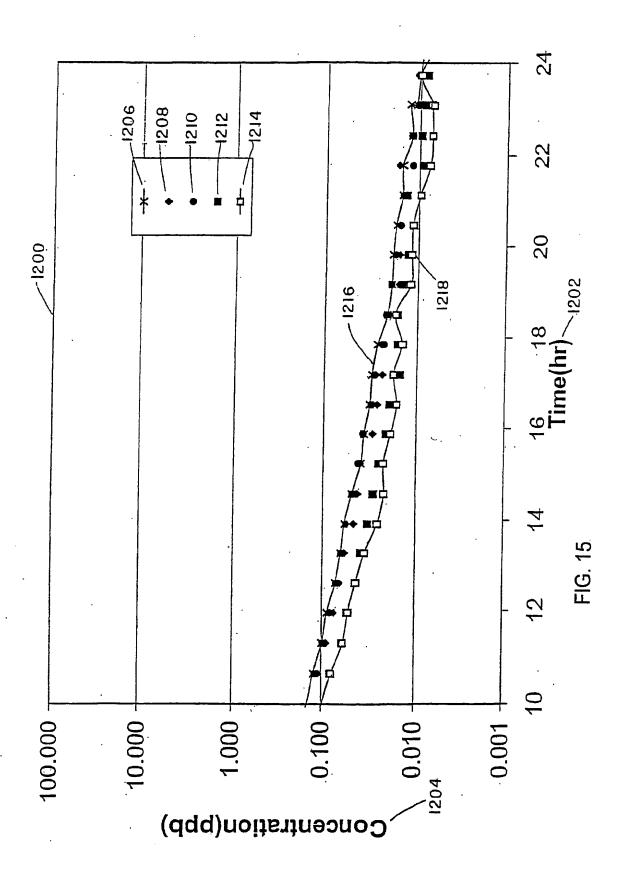












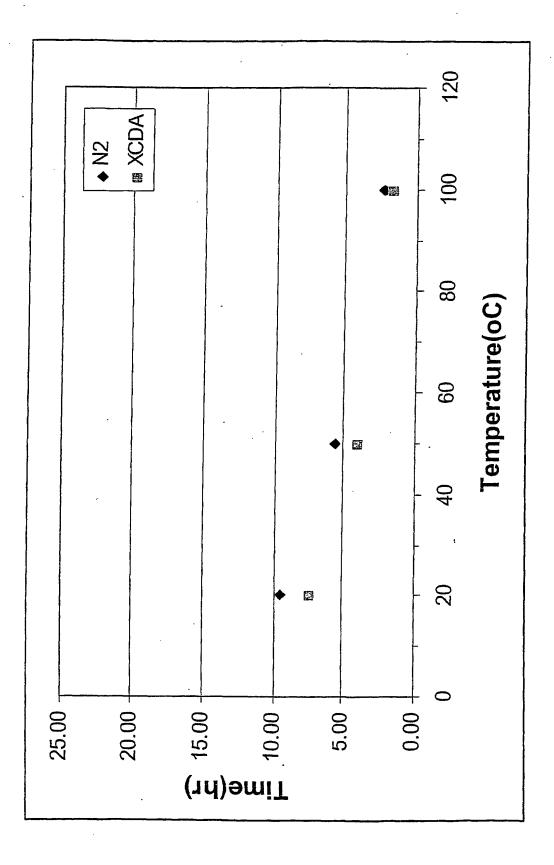


FIG. 16

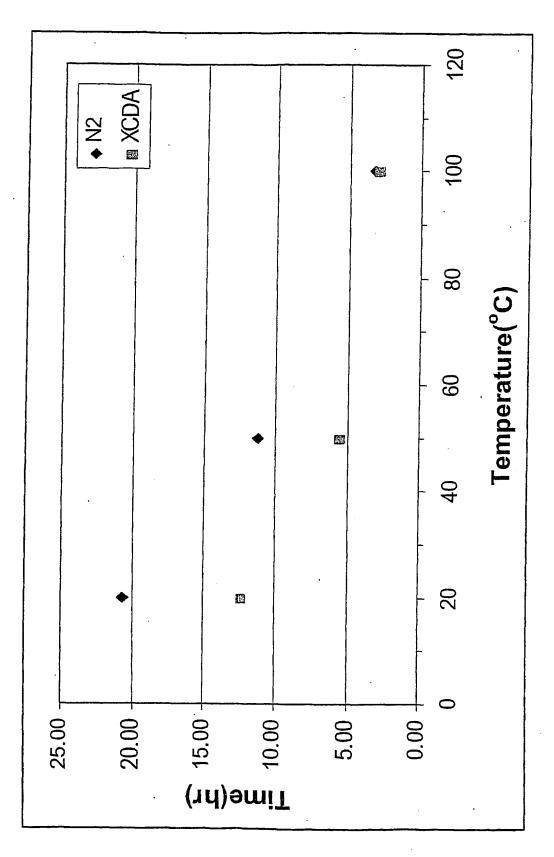


FIG. 17

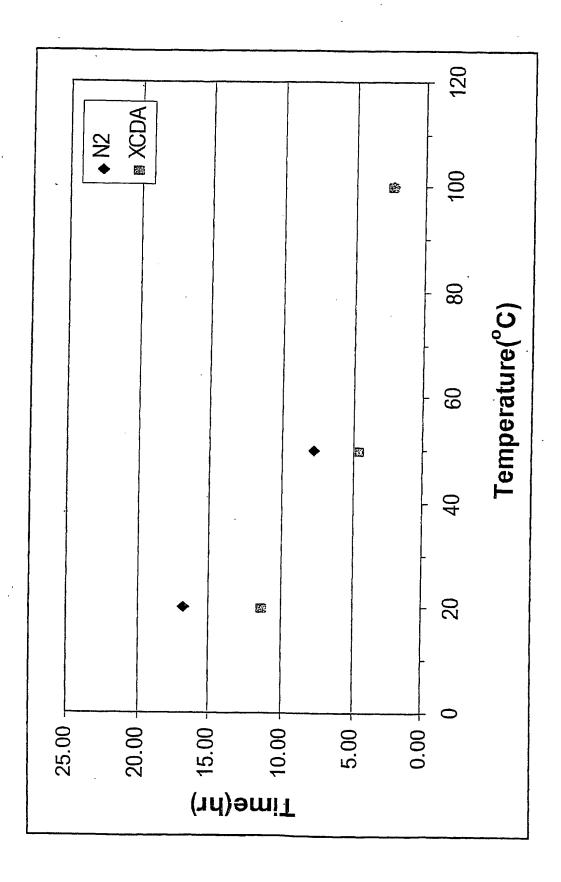


FIG. 18

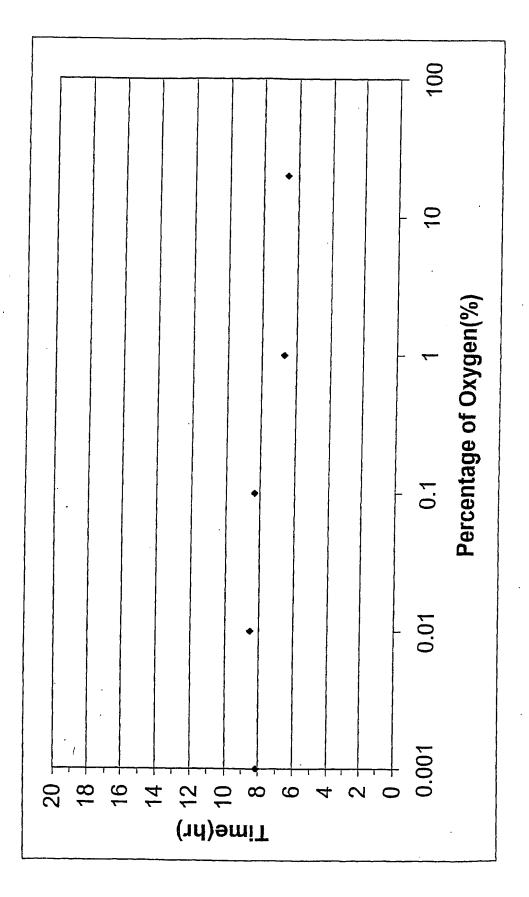


FIG. 19

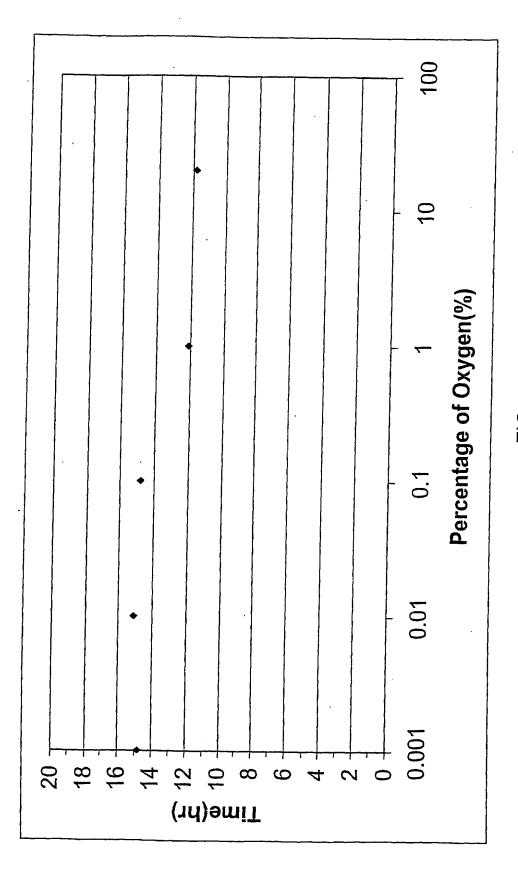


FIG. 20

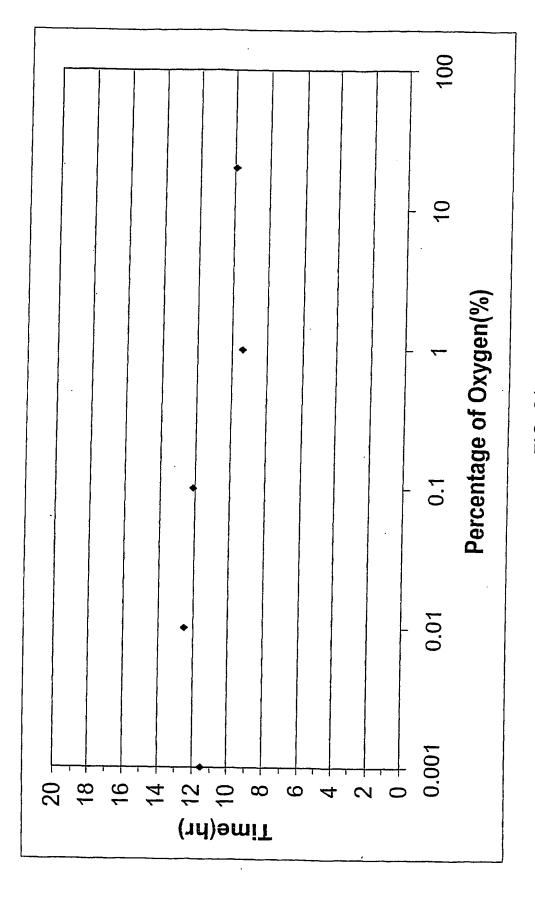
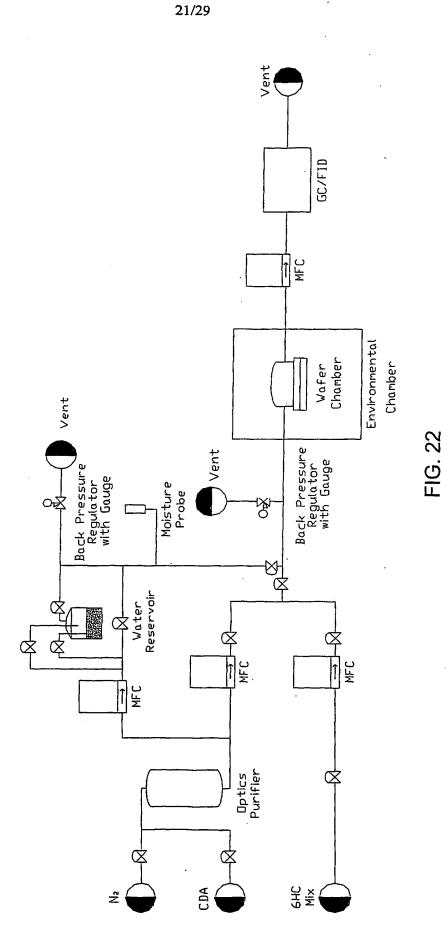
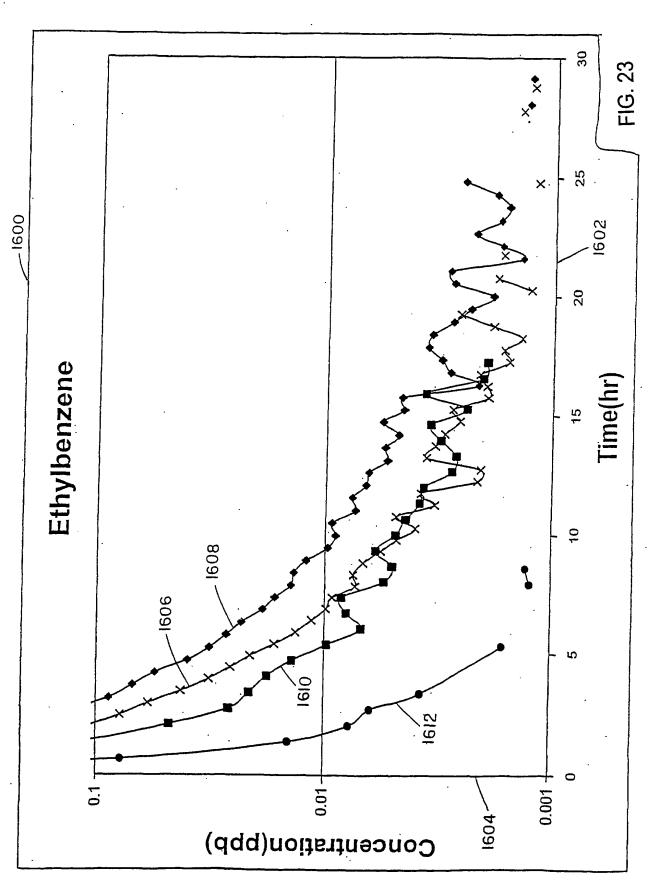
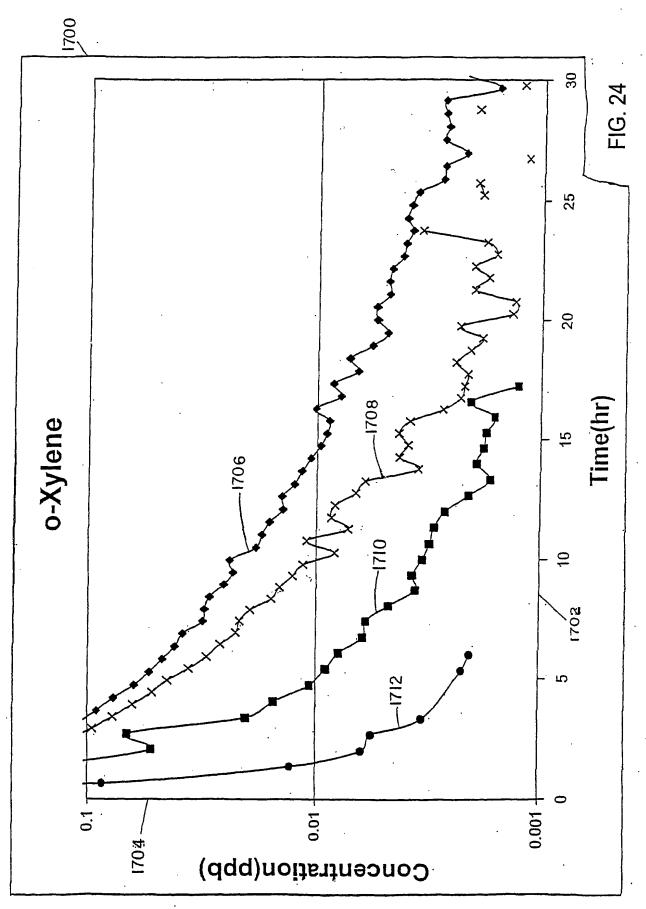


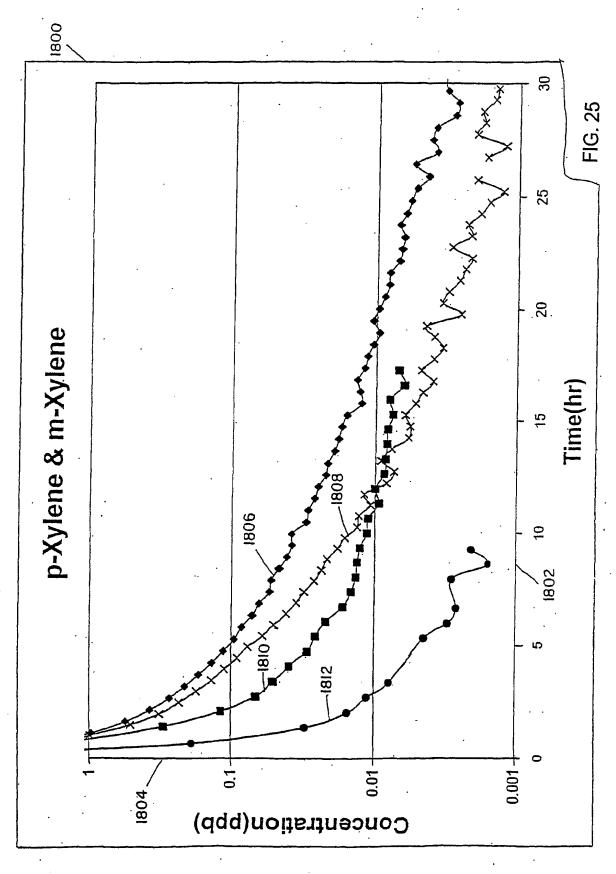
FIG. 21











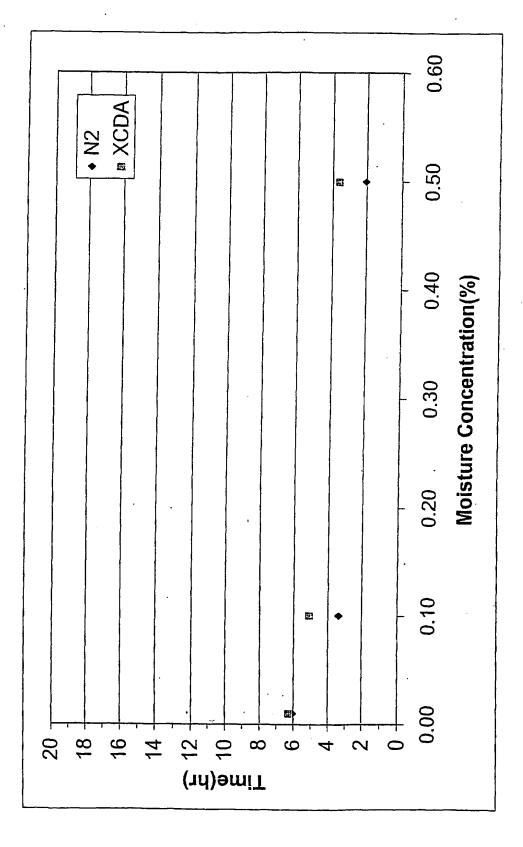


FIG. 26

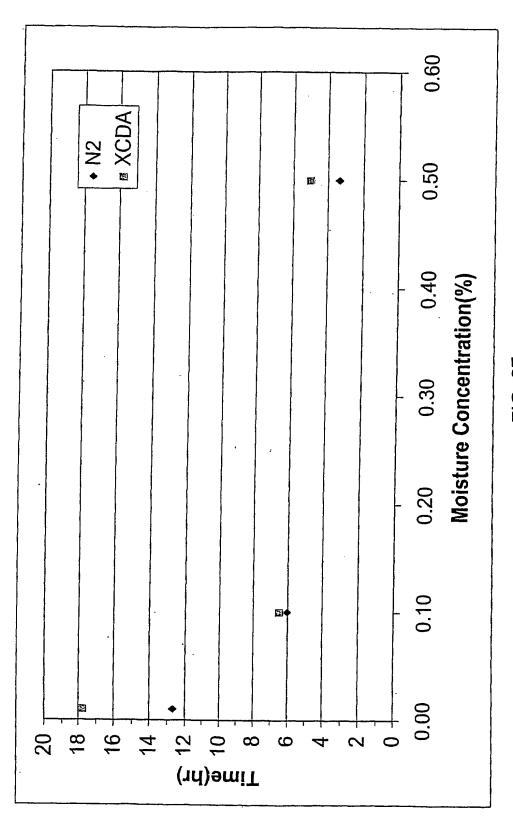


FIG. 27

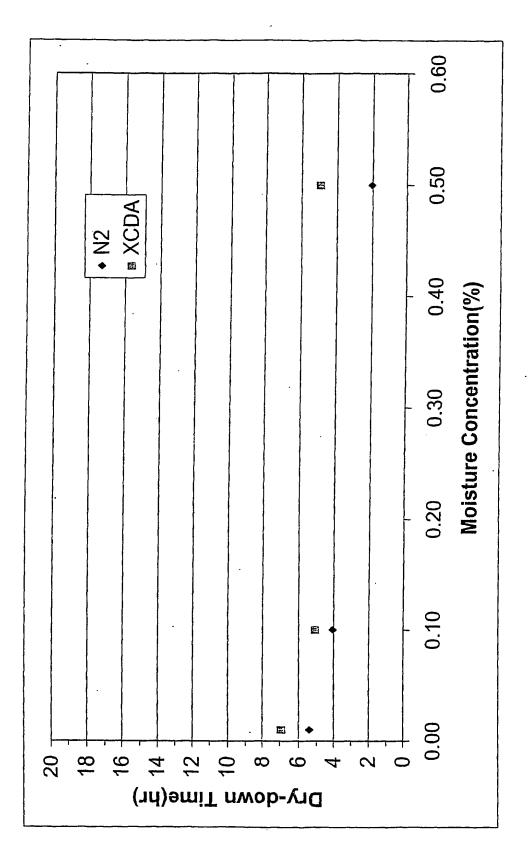
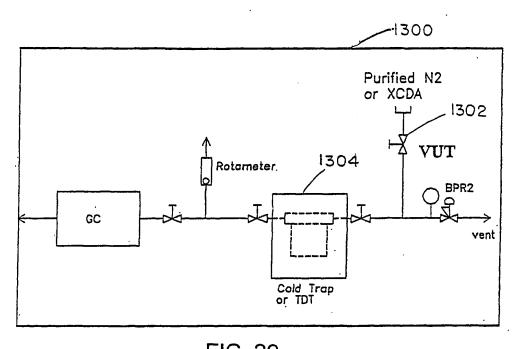


FIG. 28



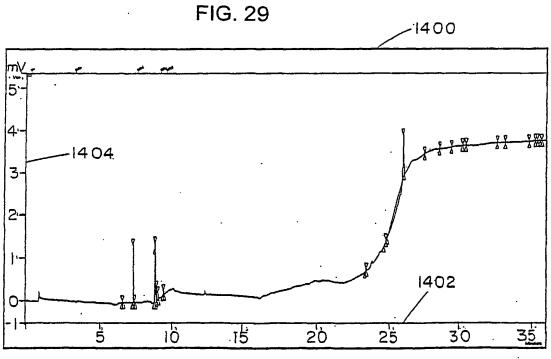


FIG. 30

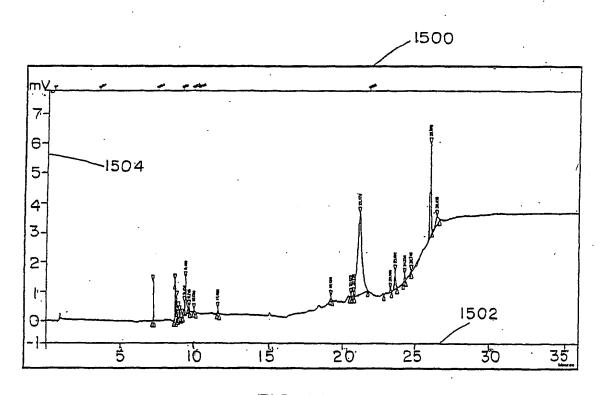


FIG. 31